The ARCtangent™-A5 Processor

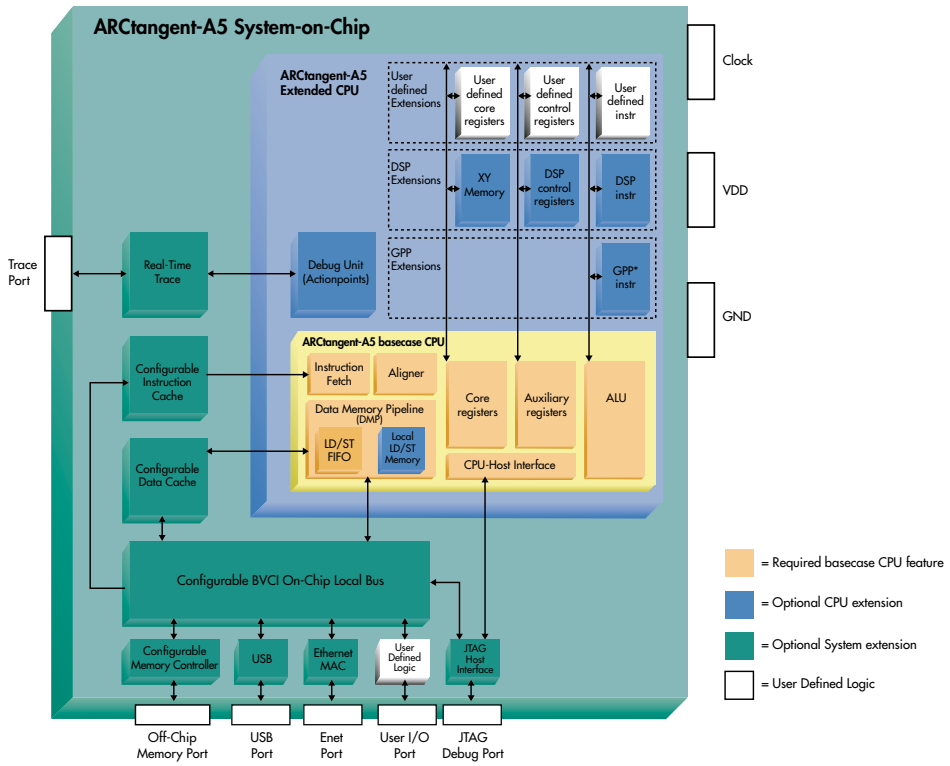
Introduction

The ARCtangent-A5 microprocessor is a user-configurable RISC/DSP core for ASIC and system-on-chip (SoC) products. It is synthesizable, configurable and extendible—developers can modify and extend the Instruction Set Architecture (ISA) for specific applications. Developers can implement the ARCtangent-A5 processor to suit different applications; areas where optimizations can be made include computational performance, I/O throughput, power consumption, silicon area and cost. ARC International customers are using the processor in a variety of applications, including set top boxes, printers, cordless phones, encryption and many other consumer devices.

As a synthesizable core delivered in HDL (Verilog® or VHDL), the ARCtangent-A5 processor can be easily ported to almost any manufacturing process, synthesis library and foundry. The ARCtangent-A5 processor is supported by easy-to-use development tools, including the ARChitect™ processor configuration tool, which has a graphical 'point-and-click' user interface.

The heart of the ARCtangent-A5 processor is a 32-bit, four-stage pipeline, RISC architecture and the ARCompact™ mixed 16/32-bit, code density optimized, instruction set. Most instructions operate in a single cycle and have optional conditional execution. The ARCompact ISA reduces code size, improves code efficiency and provides a large instruction expansion space.

For optimal code size reduction, equivalent 16-bit instructions have been implemented for the most frequently used 32-bit operations. Mixing 16 and 32-bit instructions incurs no execution penalty as there is no instruction mode switch and the processor automatically handles instructions that cross long word boundaries.



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ARCtangent-A5 Processor Feature List

CPU Architecture

- Harvard or von Neumann bus architecture
- Four-stage instruction pipeline
- 32-bit data, instruction and address buses
- BVCI protocol based interfaces
- Configurable instruction cache (1-, 2-, or 4-way, 0-32 kB)
- Configurable writeback data cache (1-, 2-, or 4-way, 0-32 kB)
- Optional on on-chip load/store RAM
- Optional 32-bit timer(s)
- 32-bit single cycle barrel shifter/rotate

ARCompact™ -ISA

- 16/32-bit instructions for high code density
- No overhead or penalty for switching instruction size
- Single-cycle instructions
- Conditional instructions (except LD/ST, 16-bit and single-operand instructions)
- Single-cycle immediate data
- Jumps and branches with single single-instruction delay slot
- Combined compare-and-branch instructions
- Delay slot execution modes
- Zero overhead loops
- Up to 128 Extension Dual or Single Operand extension Instruction Codes available

Registers

- 35 registers in base processor, extendible to 63
- 26 general purpose registers, extendible to 54
- Dedicated registers for loop count, program counter, branch link, global pointer and stack pointers
- Optional 2^{32} x 32-bit auxiliary registers (single-cycle access)

Optional Extension Instructions

- 32 x 32-bit multiplier (MUL64)
- Normalize (find first bit) instruction (NORM / NORMW)
- SWAP instruction

Optional DSP Extensions

- 24-bit multiply-accumulate (MAC)
- Dual 16 x 16-bit MAC with complex multiplication support
- Multiply subtract instruction
- ITU compliant rounding and saturating arithmetic instructions
- XY memory and address generation unit for DSP data
  - 1, 2 or 4 banks
  - 512 bytes-16kB memory size (2 blocks per bank)
  - Modulo and bit-reverse addressing
  - Variable-offset pre- and post-increment addressing modes
  - FFT/Viterbi butterfly instruction
- CRC instruction
- Division assist instruction

Power Management

- Sleep mode
- Clock Gating Option and on-chip RAM controls

Addressing Modes

- Delayed load mechanism with register scoreboard
- Pre- and post-address register write-back
- Stack pointer support
- Scaled data size addressing mode
- PC-relative addressing

Interrupts and Exceptions

- Non-maskable exceptions
- Configurable/maskable external interrupts
- 16 interrupts (extendible to 32)
- Software interrupt instruction (SWI)

Host Interface/Debug Features

- Non-intrusive on-chip debug system
- JTAG or PC parallel port interface
- Host access to register set and CPU memory
- Software breakpoints using Break or Branch instructions
- Actionpoints (hardware breakpoints)
- Optional Real Time Trace module

System Options

- Ethernet
- USB 2.0 (Hi-Speed/On-The-Go)
- UART

ISA Overview

The instruction set is orthogonal, supporting ALU and load/store operations on all general purpose registers. The ARCtangent-A5 processor provides a base set of 86 arithmetic/logical, load/store and branch/jump instructions; 35 of these instructions are 16 bits wide. Developers may define an additional 128 32-bit instructions and 128 16-bit instructions for application specific purposes.

Core Registers

The base processor has 35 core registers, 26 of which are always available for use as general purpose registers; the processor can be extended to add another 28 core registers. These extension registers can be used as general purpose registers or as specialized source/destination registers for additional instructions or logic.

DSP Extensions

Using ARChitect™, the developer can boost the computational performance of the processor by adding multiply and accumulate instructions, arithmetic instructions and on-chip XY memory with integrated programmable address generation logic for fast data access.

Auxiliary Registers

The auxiliary register set is an additional 32-bit memory space accessed with special load/store instructions, hence auxiliary register accesses do not contend with real memory accesses. The auxiliary register space can contain configuration registers that would normally be memory-mapped or occupy core-register slots.

Multiple I/O Interfaces

In addition to supporting I/O transactions through the auxiliary registers and load/store bus, the ARCtangent-A5 processor also opens up the interfaces to the core register set, ALU and condition-code unit. This allows developers to easily control the application flow, providing fast and direct access to extension functions. Developers can choose the optimal connection according to the bandwidth and latency required. The interfaces support multiple concurrent I/O transactions.

Condition Codes

The ARCtangent-A5 processor has 32 possible condition codes that can be used with most of the 32-bit instructions. The base-case processor defines the first 16 codes (00-0F), the remaining 16 codes (10-1F) are available for user extensions. Developers can define additional tests and use the results to set extension condition codes.

Software Development Tools

The ARCtangent series of processors is supported by the MetaDeveloper™ tool suite. This includes the MetaWare® C/C++ compiler, assembler, linker, profiler and the SeeCode™ debugger.

The software tool developers have worked closely with the processor design team to ensure that the toolchain has been highly optimized for the ARCtangent family of processors. The tool chain fully supports the capabilities of the ARCtangent processor including multiprocessor debugging and extensibility for processor customizations. The IDE shipped with the tools includes a sophisticated, configurable editor that can emulate popular editors such as "VI".

Software IP

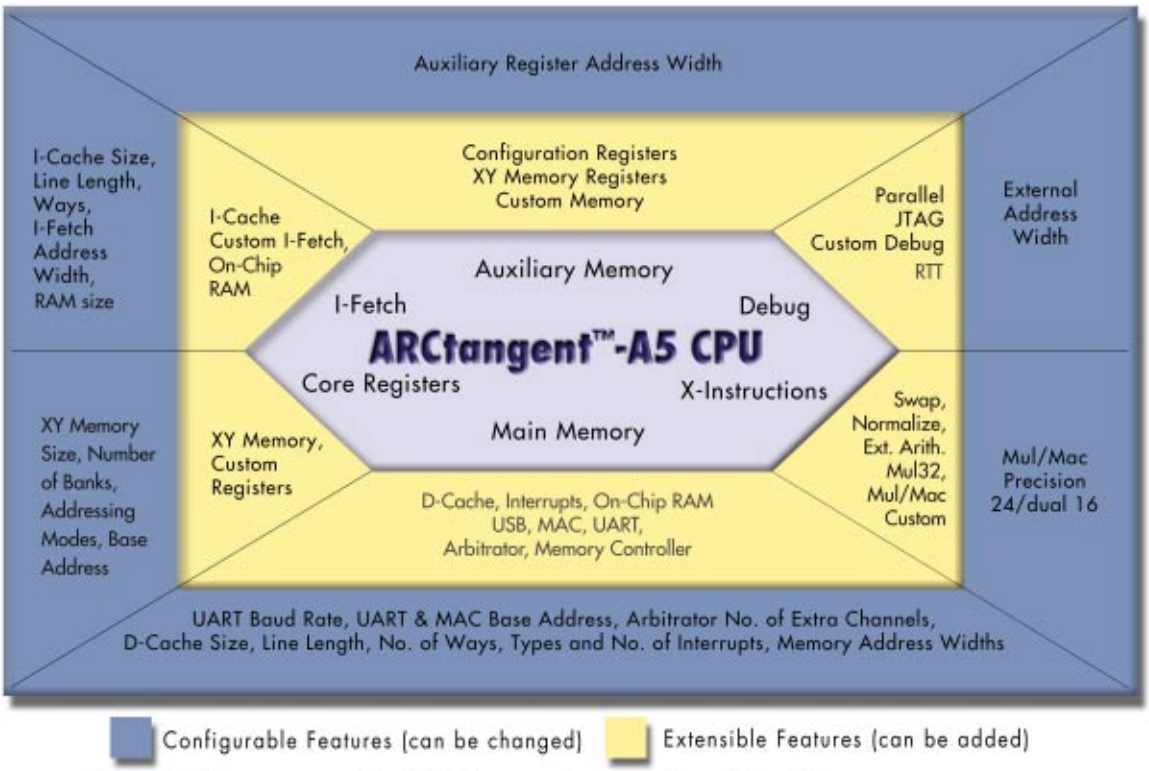
ARC International's powerful, royalty-free Precise/MQX™ RTOS is delivered with source code; it has a modular architecture to provide complete control over code footprint and feature set. ARC International also offers pre-integrated embedded middleware and protocol stacks. These are designed in a modular and efficient manner to offer the developer the power and flexibility that they require. Examples of the protocols supported include: TCP/IP, HTTP, POP3, SMTP, NAT, OSPF and IPSec.

Peripheral IP

The ARChitect tool supports the ability to integrate 10/100Mbps Ethernet Media Access Controllers (MAC), UARTs and USB 2.0 On-The-Go controllers. For systems that do not require a Hi-speed (480Mb/s) USB controller, developers can select a controller that only supports Full and Low speed transactions; this reduces the gate count of the system. Should your system not require On-The-Go functionality, Device only versions of the controllers are available. Each peripheral comes complete with Device drivers to facilitate software integration.

Real Time Trace Module

Real Time Trace is an additional extension to the ARCtangent core that enables the non-intrusive generation and transmission of information about what is happening inside the core as it is running. The information generated by a Real Time Trace system can be analyzed by the SeeCode debugger to provide instruction execution history, data movement patterns, timing information, profiling information and system level event detection. This enables comprehensive debug and profiling on application code running at full speed on a real chip or FPGA.



The ARCtangent™-A5 User-Customizable Microprocessor

Development Board

The ARCangel™ is an FPGA based flexible development board that fully supports the configurability and extensibility of the ARCtangent processor. At the heart of the ARCangel development board is a Virtex™-XCV200E FPGA; the ARChitect™ processor configuration tool can target HDL builds at this device so that developers can generate and test their processor configurations at MHz speeds. The FPGA has plenty of spare capacity for custom logic, or even more than one processor. The ARCangel also carries transceivers for peripheral IP so developers can verify their hardware solutions and software performance.

Performance

- Clock frequency (0.18µm): 170MHz
- Clock frequency (0.13µm): 230MHz
- Silicon area (0.18µm): 0.25mm^2
- Silicon area (0.13µm): 0.13mm^2

Figures were generated using typical 0.18µm and 0.13µm under worst case commercial conditions. Note that actual figures depend on the characteristics of a particular technology, operating parameters, processor configuration and synthesis constraints.

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